IN THE SPECIFICATION:

Please amend the 13th paragraph on page 5 and the 1st paragraph on page 6 as follows:

In Fig. 1, which illustrates a prior art output buffer apparatus (see: JP-A-2002-94366), a pre-buffer circuit receives a data signal D from an internal circuit (not shown), pull-up impedance adjusting signals RUP1, RUP2, ···, RUPn and pull-down impedance adjusting signals RDN1, RDN2, ···, RDNn to generate pull-up signals P1, P2, ···, Pn and pull-down signals D1, D2, ···, Dn. The pull-up signals P1, P2, ···, Pn and the pull-down signals D1, D2, ···, Dn are supplied to a main-buffer circuit 2 which, in turn, generates an output signal[[s]] at the output terminal OUT.

The pull-up impedance adjusting signals RUP1, RUP2, ···, RUPn and the pull-down impedance adjusting signals[[,]] RDN1, RDN2, ···, RDNn are generated from an impedance adjusting generating circuit 3 which is constructed by a control circuit 31, a dummy pre-buffer circuit 32, a dummy main-buffer circuit 33, a comparator 34 and switches 35 and 36. In this case, the dummy pre-buffer circuit 32 and the dummy main-buffer circuit 33 have the same circuit configuration as the pre-buffer circuit 1 and the main-buffer circuit 2, respectively. In this case, the dummy pre-buffer circuit 32 receives a dummy data signal D' and pull-up impedance adjusting signals RUP1', RUP2', ···, RUPn', and pull-down impedance adjusting signals RDN1', RDN2', ···, RDNn' from the control circuit 31. Also, the switches 35 and 36 formed by MOS transistors are controlled by the control circuit 31. Further, a resistor 4 is externally connected between the output of the dummy main-buffer circuit 33 and a node of the switches 35 and 36. Note that the resistor 4 can be internally provided in the output buffer apparatus of Fig. 1. In this

case, the resistance value of the resistor 4 corresponds to the characteristic impedance of a transmission line to be connected to the output terminal OUT.

Please amend the 1st paragraph on page 7 and the 2nd paragraph on page 8 as follows:

For example, as illustrated in Fig. 3A, when the pull-up impedance adjusting signal PUPi (PUPi') is "1" (high) and the data signal D (D') is "0" (low), the transfer gates 101 and 102 are turned ON and OFF, respectively, so that the pull-up signal Pi (Pi') is low (activating level). On the other hand, when the pull-up impedance adjusting signal PUPi (PUPi') is "1" (high) and the data signal D (D') is "1" (high), the transfer gates 101 and 102 are turned OFF and ON, respectively, so that the pull-up signal Pi (Pi') is high (deactivating level). Note that, if the data signal D (D') is high, the pull-up signal Pi (Pi') is high (deactivating level) regardless of the pull-up impedance adjusting signal ~~PUPi (PUPi')~~ RUPi (RUPi').

Similarly, as illustrating in Fig. 3B, when the pull-down impedance adjusting signal ~~PDNi (PDNi')~~ RDNi (RDNi') is "1" (high) and the data signal D (D') is (high), the transfer gates 105 and 106 are turned ON and OFF, respectively, so that the pull-down signal Ni (Ni') is high (activating level). On the other hand, when the pull-down ~~pull-up~~ impedance adjusting signal ~~PUPi (PUPi')~~ RUNi (RUNi') is "1" (high) and the data signal D (D') is low, the transfer gates 105 and 106 are turned OFF and ON, respectively, so that the pull-down signal Ni (Ni') is low (deactivating level). Note that, if the data signal D (D') is low, ~~high~~ the pull-down signal Ni (Ni') is low (deactivating level) regardless of the pull-down impedance adjusting signal ~~PDNi (PDNi')~~ RDNi (RDNi').

Please amend the 4th paragraph on page 8 as follows:

For example, as illustrated in Fig. 5, when the pull-up signal Pi (Pi') is low (activating level) and the pull-down signal Ni is low (deactivating level), the transistors 201 and 202 are turned ON and OFF, respectively, so that the voltage at the output terminal OUT is high. On the other hand, when the pull-up signal Pi (Pi') is high (deactivating level) and the pull-down signal Ni is high (activating level), the transistors 201 and 202 are turned OFF and ON, respectively, so that the voltage at the output terminal OUT is low. Note that the pull-up signal Pi (Pi') and the pull-down signal Ni (Ni') are never at the activating levels simultaneously, i.e., which is forbidden. Also, when the pull-up signal Pi (Pi') is high (deactivating level) and the pull-down Ni (Ni') is low (deactivating ~~activating~~ level), the output terminal OUT is in a high impedance (HZ) state.

Please amend the 2nd paragraph on page 9 as follows:

The calibrating operation of the impedance adjusting circuit 3 of Fig. 1 will be explained next with reference to Figs. 6, 7A and 7B. Here, impedance codes RUP, RDN, RUP' and RDN' are defined by

RUP = (RUPn, RUPn-1, ···, RUP1)

RDN = (RDNn, RDNn-1, ···, RDN1 ~~PDN1~~)

RUP' = (RUPn', RUPn-1', ···, RUP1')

RDN' = (RDNn', RDNn-1', ···, RDN1' ~~PDN1'~~)

Please amend the 4th paragraph on page 11 and the 1st paragraph on page 12 as follows:

The D-type flip-flop 1i-1 (i = 1, 2, ···, n) has a data input D for receiving the pull-up impedance adjusting signal RUPi, a clock terminal C for receiving the data signal D and an output terminal Q for generating an output signal which is transmitted to the inverter 103 of the pre-driver 1i. That is, the pull-up impedance adjusting signal RUPi ~~PUPi~~ is fetched by the D-type flip-flop 1i-1 in synchronization with a falling edge of the data signal D.

The D-type flip-flop 1i-2 (i = 1, 2, ···, n) has a data input D for receiving the pull-down impedance adjusting signal RDNi, a clock terminal C for receiving an inverted signal of the data signal D and an output terminal Q for generating an output signal which is transmitted to the inverter 105 of the pre-driver 1i. That is, the pull-down impedance adjusting signal RDNi ~~PDNi~~ is fetched by the D-type flip-flop 1i-2 in synchronization with a rising edge of the data signal D.

Please amend the 2nd and 3rd paragraphs on page 15 as follows:

That is, the impedance code RUP is fetched at periods t2 to t3, t4 to t5, t6 to t7, t8 to t8', t10 to t11, t12 to t13, t14 to t15, t16 to t17 when the data signal D is "0" (low). On the other hand, the impedance code RDN ~~RDP~~ is fetched at periods t1 to t2, t3 to t4, t5 to t6, t7 to t8, t9 to t10, t11 to t12, t13 to t14, t15 to t16 when the data signal D is "1" (high).

In the calibrating operation as illustrated in Fig. 16, when the impedance code RUP ~~RUN~~ is changed as indicated by Y1, Y2, ··· in Fig. 16 while the data signal D continues at the value "0" (low), the changed code RUP ~~RUN~~ is fetched, and also, when the impedance code RDN ~~RDP~~ is changed as indicated by Z1, Z2, ··· in Fig. 16 while the data signal D continues at the value "1" (high), the changed code RDN ~~RDP~~ is fetched. Therefore, a discrepancy between the

output impedance of the output buffer apparatus and the characteristic impedance of the transmission line may be suppressed which would suppress reflection noise at the terminal of the transmission line.